Custom Circuit Solutions

FIM-EP3C5 Manual

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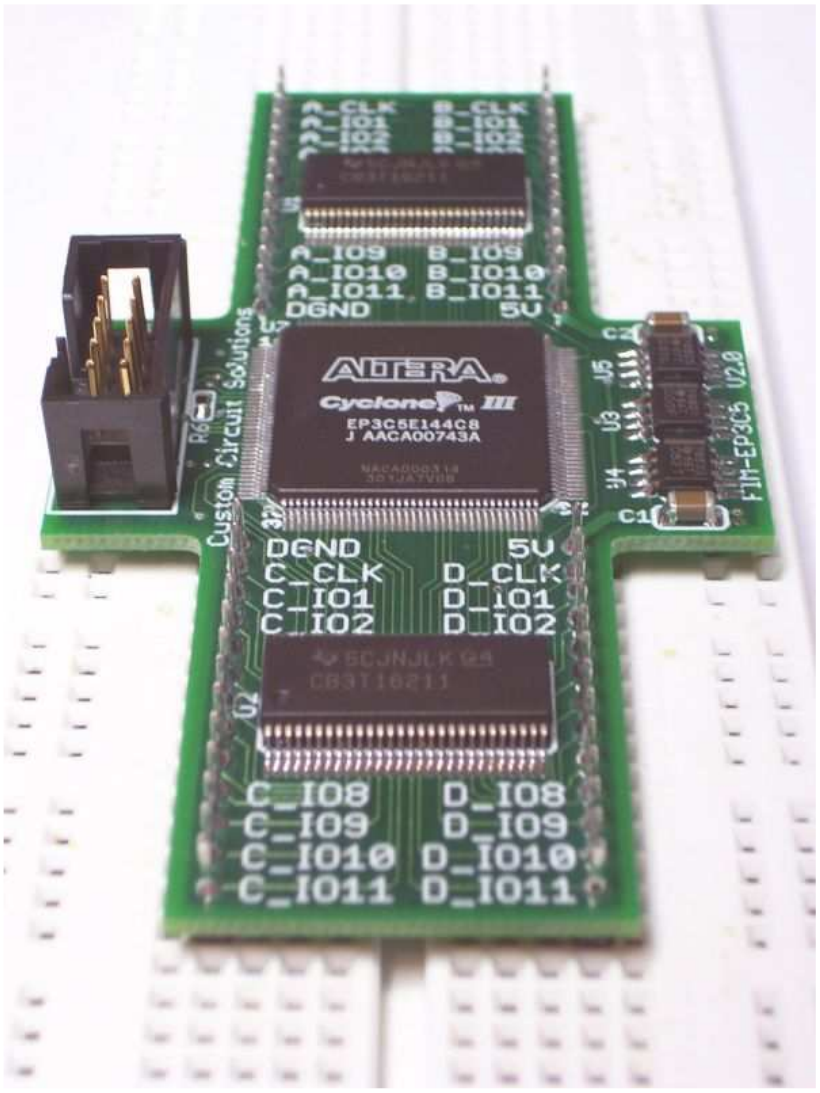

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1.0 Overview – The FIM-EP3C5 is an integrated module based on the Altera Cyclone-III FPGA. It integrates everything needed to quickly add the industry's most advanced FPGA technology to a prototype or test circuit. Each module provides a complete digital solution in a DIP package, allowing it to be added to most any breadboard or wire-wrap application. The benefits of these modules include:

- **Complete digital solution in a single small package (logic gates, RAM, PLLs, ...)**
- **Requires only a single 5V power supply for operation**
- **I/O pins compatible with most 5V, 3.3V, and 2.5V logic systems**
- **20MHz reference clock and PLLs allow for complex clocking solutions**
- **DIP packaging allows quick installation into most prototyping boards**
- **Significantly reduce time, money, and headaches in wiring a prototype circuit**
- **Display all I/O pin signals and nearly all internal FPGA signals with the use of the JTAG port and Altera's FREE SignalTap-II logic analyzer software**

1.1 Specifications

Feature	Description
FPGA	Altera Cyclone-II EP3C5-8 (contact us for different size and speed grades)
Logic Elements	5,136
Total RAM Bits	423,936
Embedded 18x18 Multipliers	23
Phase Locked Loops	2
User I/O Pins	44
Dedicated Clock/Input Pins	4
Integrated Clock	20MHz (Higher frequencies synthesizable using one of the PLLs)
Debug and Programming Port	10-Pin JTAG Header (Compatible with Altera's ByteBlaster-II and USB-Blaster cables)
Allowable Input Voltage Levels	5.0V, 3.3V, and 2.5V
Output Pin Characteristics	3.3V @ 8mA max source/sink *
Max Operating Frequency	125MHz to 300MHz Typical (Function Dependant - Please see Altera's Cyclone-III documentation)
Power Requirements	5V @ .1A typical
Packaging	DIP - .1" Headers
Physical Dimensions	3.7" x 2.1"

*Compatible with most 5V, 3.3V, and 2.5V logic systems. Check with interfacing component manufacturer for compliance.

For more detailed specifications of the Altera Cyclone-III device, please see www.altera.com.

PLEASE READ PRIOR TO INSTALLING

2.0 Installation and Removal – Please read prior to installation, failure to do so may result in damages to the module. Any damages found to have occurred as the result of failing to properly follow these guidelines will not be covered under Custom Circuit Solutions warranty.

Like any DIP package, care must be given to protect the device during installation and removal. Excessive torque or pressure applied on the board may damage the circuitry and bend the pins. Also, careful planning should be taken prior to installing the module to limit the number of installation and removal cycles needed.

2.1 Installation – Before installing, pick an appropriate location for the device. The pin columns of the FIM module are spaced 0.9 inches apart. DO NOT try to install the device in any spacing other than 0.9 inches as this will likely bend the pins. While it can be installed in many numerous configurations, it is intended to be placed in the middle of a standard (5 pin row, 2 columns, N rows) breadboard strip. This will leave the outer pins of the breadboard columns open for connections.

Once the module has been set in the desired location, check that all pins properly line up in the breadboard holes prior to applying any pressure. Once all pins are properly aligned, apply pressure to the module at the locations shown in blue in Figure 1. DO NOT apply pressure directly to any of the topside components as this may damage them or their solder connections. Excessive force should not be used to install the module. If the module does not want to insert easily, recheck the pin alignment. With moderate pressure, fully insert the unit into the breadboard.

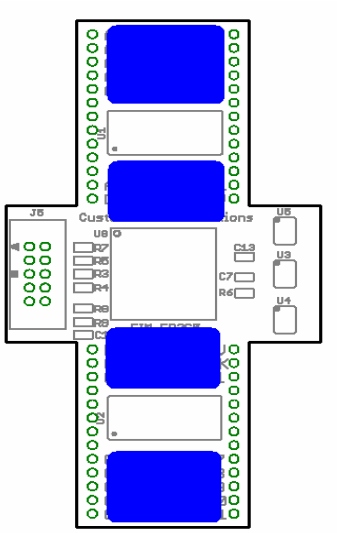

Figure 1: Installation Points

2.2 Removal – Proper care must be taken when removing the unit from a breadboard. To remove the unit, a flat head screwdriver should be used to gently raise each corner of the module at the points shown in Figure 2. DO NOT try to fully remove one corner of the device from the breadboard before raising the other corners. Instead, carefully raise one corner approximately 1/8th of an inch. Then, move to another corner and raise it the same amount. Once all corners have been raised an equal amount, restart the process until the module easily lifts from the breadboard. DO NOT attempt to lift the board at any locations other than those shown in Figure 2. There are components on the bottom side of the board that can be easily damaged. Additionally, lifting from the side tabs of the board can easily torque the board, causing damage to the components.

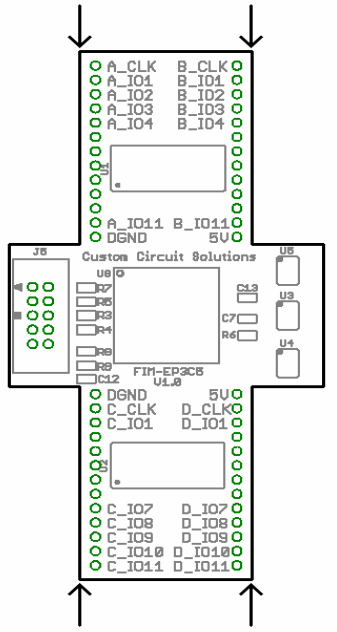

Figure 2: Removal Points

3.0 Setup and Configuration – The following sections provide information on how to operate the FIM-EP3C5.

3.1 Power Connections – The FIM module requires a single 5V power supply for operation. There are two 5V pins and two ground "DGND" pins on the module. These pins are labeled on the topside of the board. All four of these pins must be connected to the proper voltages. Failure to do so may damage the module.

3.2 Programming Port – Programming of the FIM module is done through the 10-pin JTAG port header (J5). This header is compatible with both Altera's ByteBlaster-II and USBBlaster programming cables. Third party programmers may also be used.

There are two options for programming the FIM module. The first option is to program the FPGA device only using the JTAG port and an ".sof" file. This is the fastest option for programming the module. However, PLEASE NOTE that this option is volatile and upon power cycling of the device, the configuration will be lost.

The second option for programming of the module is using the JTAG port and an Altera JTAG Indirect Configuration (JIC) file. The JIC file programming method should be used in order to reprogram the module's non-volatile EPCS4 configuration device. A ".jic" file can be created from an ".sof" file using the Quartus-II "Convert Programming Files" dialog. Custom Circuit Solutions provides Quartus-II programming environment templates, which are documented in section 3.4, that contain a conversion setup file ".cof" for properly generating the ".jic" files. For additional programming details please contact Custom Circuit Solutions or see Altera's Cyclone-III Device Handbook.

3.3 IO Pins – Each FIM-EP3C5 module has four banks of IO pins. These four banks are labeled A, B, C, and D. Each bank has 11 IO pins and 1 dedicated global clock pin. The global clock pin may also be used as a general input pin. Some of the pins are labeled on the top side of the module for quick reference.

Connected to each IO pin is a voltage translation circuit that clamps the voltage passed to the FPGA to 3.3V. This allows 5V circuitry to drive the module. NOTE that if an IO pin is programmed to a high impedance state "Z", the pin voltage will float at approximately 3.3V due to this circuitry. If a high impedance state of a pin is utilized, it is recommended that the user add either a pull up or pull down resistor, external to the module.

The FPGA IO pins are configured to operate at 3.3V, with a maximum source/sink capability of 8mA. This allows the module to directly interface to 5V TTL, 3.3V LVTTL, and 3.3V LVCMOS. It can also interface directly to 5V CMOS devices if the inputs are 5V TTL level compatible, as most new devices are. If not, a 1K ohm pull-up resistor to 5V is required, and the IO pin should be set to a high impedance "Z" state to output a logic high. Likewise, the FIM module can directly drive 2.5V CMOS devices if the inputs are 3.3V tolerant. If not, the IO pin should be pulled up to 2.5V using a 1K ohm resistor, and set to a high impedance state for a logic high. PLEASE check the specifications of any components that interface to the FIM module for compatibility. Custom Circuit Solutions does not assume any liability for components damaged by incompatibilities.

While both the Cyclone-III device and the voltage translation circuit can safely source or sink 8mA, some limitations apply. The high output impedance of the translation circuitry can cause the IO pin output voltage to sharply drop while sourcing a significant amount of current, starting around 1mA. The current sinking ability of the FIM module is not affected the same way. As a result, it is recommended that the current sinking ability of the device be used rather than its sourcing. For example, to drive an LED output, do not ground the cathode and drive the anode high using an IO pin, as seen in Figure 3. This can lead to an IO voltage less than the specified 3.3V. Rather, connect the anode to the desired supply voltage and drive the cathode low, shown in Figure 4. This issue should not be a concern when interfacing to other TTL or CMOS pins as the input impedance is sufficiently large, and thus draws low output currents. However, if the fan-out or fan-in is too great, this issue should be monitored. Please contact Custom Circuit Solutions for additional help in this matter.

It is recommended that all pins configured as outputs be set to utilize the minimum required drive current. These changes can be made through the Quartus-II "Assignment Editor." Cyclone-III devices have fast rise and fall times on their output pins which can create excessive signal ringing if not properly terminated. In addition, if multiple pins are switching and ringing simultaneously, this can lead to power supply noise within the module. By reducing the drive current of the output pins, signal ringing is minimized.

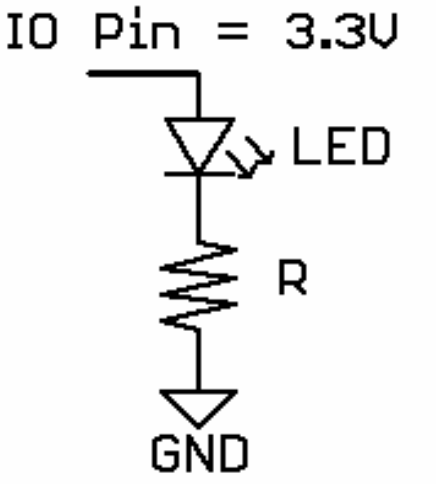

Figure 3: Improper LED Driving Method

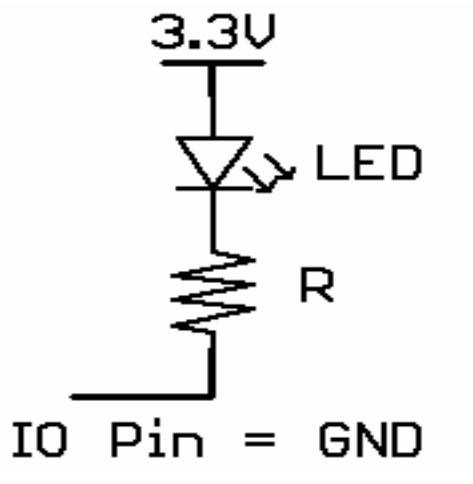

Figure 4: Preferred LED Driving Method

In the Quartus-II programming templates provided by Custom Circuit Solutions, the module IO pins have already been assigned to the Cyclone-III device pins. However, if third party programming software is used or if a change of IO pin names is desired within Quartus-II environment, the user must remap the pins. The following table provides the module pin to FPGA pin mapping.

The 20MHz clock is provided on FPGA pin 91.

Module Pin	FPGA Pin	Module Pin	FPGA Pin	Module Pin	FPGA Pin	Module Pin	FPGA Pin
A_CLK	129	B_CLK	52	C_CLK	24	D_CLK	88
A_IO1	132	B_IO1	125	C_IO1	39	D_IO1	68
A_IO2	133	B_IO2	121	C_IO2	33	D_IO2	69
A_IO3	135	B_IO3	120	C_IO3	32	D_IO3	71
A_IO4	136	B_IO4	119	C_IO4	31	D_IO4	72
A_IO5	137	B_IO5	115	C_IO5	42	D_IO5	67
A_IO6	141	B_IO6	114	C_IO6	43	D_IO6	66
A_IO7	142	B_IO7	113	C_IO7	44	D_IO7	65
A_IO8	7	B_IO8	106	C_IO8	46	D_IO8	64
A_IO9	4	B_IO9	110	C_IO9	49	D_IO9	60
A_IO10	144	B_IO10	111	C_IO10	50	D_IO10	59
A_IO11	143	B_IO11	112	C_IO11	51	D_IO11	58

Table 1: FIM-EP3C5 Pin to Cyclone-III Pin Mapping

3.4 Quartus-II Templates – The FIM-EP3C5 module can be programmed using Altera's free Quartus-II software, version 7.2sp1 or greater. Custom Circuit Solutions provides preconfigured Quartus-II programming templates to speed application development. These templates contain all necessary files, pin configurations, and programming parameters. Both VHDL and schematic entry templates are available so that the user can program in whatever method they feel comfortable with.

To utilize a Quartus-II programming template, start by downloading the appropriate file from the Custom Circuit Solutions website. If you wish to program using VHDL, download the VHDL zip file. If you prefer to program using a schematic entry method, download the schematic zip file. Unzip the downloaded file to the desired location. Click on the Quartus-II project file "EP3C5.qpf". This will bring up Quartus-II and load the project settings. If you are working with the VHDL environment, open the "EP3C5.vhd" file. If you are using the schematic entry environment, open the "EP3C5.bdf" file.

The following is a list of files contained in the zip.

- README.txt – This file contains some important notes regarding the default configuration of the templates.
- EP3C5.vhd – VHDL code template with all necessary IO pin declarations and a preconfigured PLL for common clock frequencies. Users should add their custom code to this file if working in VHDL.
- EP3C5.bdf – Schematic entry template with all necessary IO pin declarations and a preconfigured PLL for common clock frequencies. Users should add their custom schematics to this file.
- EP3C5.stp – SignalTap-II file with all IO pins pre-entered for easy monitoring. Users can adjust acquisition parameters and add custom signals to be monitored.
- EP3C5.cdf – Programmer configuration file. This file should be modified based upon programming requirements. For a fast volatile programming of the FPGA only, set this to use the ".sof" file. For a slower non-volatile programming of the EPCS4 configuration device, set this to use the ".jic" file.
- EP3C5.qsf – The Quartus-II settings file contains all of the device parameters and IO pin mappings.
- EP3C5.cof – This file is the configuration setup file for quickly generating a ".jic" programming file from a ".sof" file.

All that is left to the user is to add logic, compile, and download. This of course assumes some prior knowledge of the Quartus-II software. Please contact either Custom Circuit Solutions or Altera for additional help in using the Quartus-II software.